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EXAMINER	
RUTZ, JARED IAN	

ART UNIT	PAPER NUMBER
2187	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/27/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/631,205	CHAUVEL ET AL.	
	Examiner	Art Unit	
	Jared I. Rutz	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 December 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14 and 16-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14 and 16-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-14, and 16-20, as amended on 12/13/2006, are pending in the instant application. Applicant's Arguments submitted 12/13/2006 have been carefully and fully considered, but are considered moot in light of the new grounds of rejection presented in this Office action. As the new grounds of rejection presented in this Office action were necessitated by amendment, this Office action is made **FINAL**.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. **Claims 1-8** are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

4. **Claim 1** has been amended to recite the limitation "*determining whether the data is being removed from a dirty cache line in a cache memory*". The Examiner is not aware of a portion of the specification which teaches determining whether the data is being removed from a dirty cache line in a cache memory.

5. **Claims 2-8** depend from claim 1, and are rejected for the same reasons as claim 1.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. **Claims 1-8** are rejected under 35 U.S.C. 103(a) as being unpatentable over Adams, III et al. (US 6,151,661) in view of Lopriore (Line fetch/prefetch in a stack cache memory) and Handy (The Cache Memory Book).

8. **Claim 1** is taught by Adams as:

a. *A method of managing memory, comprising: issuing a data request to remove data.* Column 4 lines 55-56 show a POP operation issued by processor 12.

9. Although Adams teaches that the cache memory is used for stack and non-stack data (Adams column 4 lines 26-29), Adams does not explicitly teach determining whether the data is being removed from a dirty cache line, stating that non-stack operations are managed by known computing procedures (Adams column 4 lines 31-33).

10. With respect to claim 1, Handy teaches

b. *Determining whether the data is being removed from a dirty cache line in a cache memory.* Page 66 lines 22-24 show that during a cache miss cycle, the line to be replaced is examined, and if its Dirty bit is set the current contents of that cache line are evicted back to main memory.

11. Adams and Handy are analogous art because they are from the same field of endeavor, computer data cache design.

12. At the time of the invention it would have been obvious to a person of ordinary skill in the art to check if the data being removed from the cache of Adams is from a dirty cache line.

13. The motivation for doing so would have been to make sure valid, changed data is written back to main memory, and therefore not lost, while reducing main memory accesses (Handy page 65 lines 22-30).

14. Therefore, it would have been obvious to combine Handy with Adams for the benefit of maintaining changed data when it is removed from the cache to obtain the invention as specified in claims 1-8.

15. With respect to claim 1, Adams further teaches:

c. *And if the data being removed corresponds to a predetermined word in the dirty cache line, queuing the dirty cache line for replacement.* Adams at column 4 line 66 through column 5 line 6 shows that if the data word to be popped is the highest address word in the cache line, the other words in the cache line are necessarily invalid, and the processor is instructed to invalidate the cache line.

When the cache line is invalidated, it is left empty and made available for other valid data.

16. Adams teaches that if the data word to be POPPED is the highest address word in the cache line, that word is the last possible word to be POPPED in that particular cache line and the entire cache line is invalidated (column 5 lines 2-4). Adams also states that the cache line is made available for other valid data (column 5 lines 4-6) Adams makes no exceptions for dirty/not dirty lines. However, Adams does not explicitly teach that a dirty cache line is invalidated, or that the invalidated cache line is not written to memory after POPPING the highest address word of a cache line.

17. With respect to claim 1, Lopriore teaches:

d. *And not writing the dirty cache line to a memory external to a processor.* In the third paragraph of the second column of page 547, which continues on page 548, Lopriore states "*when the stack shrinks, the cache lines reserved for the discarded stack portions at the stack top become free. The cache contains no valid information for these lines, so we do not have to copy the contents of these lines to the primary memory*"

18. The combination of Adams and Handy and Lopriore are analogous art because they are from the same field of endeavor, computer data cache design.

19. At the time of the invention it would have been obvious to a person of ordinary skill in the art to not write a dirty cache line to main memory when the highest address word in the cache line is POPPED, as the cache line does not contain any valid data

(Adams column 5, lines 2-4; Lopriore page 547, second column, line 39 through page 548, first column, line 2).

20. The motivation for doing so would have been to save unnecessary writes to main memory (Lopriore page 547, second column, lines 1-14; also a goal of Adams, column 1 line 54 through column 2 line 11).

21. Therefore, it would have been obvious to combine Lopriore with Adams and Handy for the benefit of eliminating unnecessary memory cycles to obtain the invention as specified in claims 1-8.

22. **Claim 2** is taught by Adams as:

e. *The method of claim 1, wherein the predetermined word is the first word in the dirty cache line*. Column 4 line 66 to column 5 line 6 shows that if the popped data word is the highest address word in the cache line, the processor invalidates the cache line. As shown in figure 2, in the direction of a push operation the highest address word is first in the cache line.

23. **Claim 3** is taught by Adams as:

f. *The method of claim 2, wherein the dirty cache line is invalidated*. Column 4 line 66 to column 5 line 6 shows that if the popped data word is the highest address word in the cache line, the processor invalidates the cache line.

24. **Claim 4** is taught by Handy as:

g. *The method of claim 2, wherein the dirty cache line is queued for replacement by a replacement policy when a read hit occurs on the first word of the dirty cache line.* With respect to claim 4 Handy teaches that if the cache is a multi-way cache, an algorithm must be used to select a line to be replaced, page 57 lines 3-14.

25. At the time of the invention it would have been obvious to use a multi-way set associative cache in the system of Adams.

26. The motivation for doing so would have been to lessen thrashing while still improving the hit rate over a direct mapped cache, Handy page 54 lines 1-18.

27. Therefore it would have been obvious to combine the multi-way set associative cache of Handy with Adams for the benefit of reducing thrashing while improving hit rate to obtain the invention as specified in **claims 4-5**.

28. **Claim 5** is taught by Handy as:

h. *The method of claim 4, wherein the replacement policy is a least recently used (LRU) policy.* Page 57 lines 10-14 teaches the use of a LRU replacement algorithm.

29. **Claim 6** is taught by Adams as:

i. *The method of claim 1, wherein the predetermined word is the last word in the dirty cache line.* Column 4 line 66 to column 5 line 6 shows that if the popped data word is the highest address word in the cache line, the processor invalidates

the cache line. As shown in figure 2, in the direction of a pop operation the highest address word is the last word in the cache line.

30. **Claim 7** is taught by Handy as

j. *The method of claim 1, wherein queuing the dirty cache line for replacement comprises designating the dirty cache line as least-recently-used (LRU).* Page 57 lines 9-10 state "*Ideally, any stale piece of cached data which is no longer needed by the processor would be chosen to be overwritten.*" As the cache line is invalidated when the highest address word in the cache line is popped, that cache line no longer contains data which is needed by the processor. At the time of the invention, it would have been obvious to one of ordinary skill in the art to designate the invalidated dirty cache line for replacement. The motivation for doing so would have been to prevent evicting useful data, which may still be useful to the processor, from the cache.

31. **Claim 8** is taught by Adams as:

k. *The method of claim 1, further comprising invalidating the dirty cache line if the predetermined word in the dirty cache line is the first word.* Column 4 line 66 to column 5 line 6 shows that if the popped data word is the highest address word in the cache line, the processor invalidates the cache line. As shown in figure 2, in the direction of a push operation the highest address word is first in the cache line.

32. **Claims 9-11, 14, 16-18, and 20** are rejected under 35 U.S.C. 103(a) as being unpatentable over Adams, III et al. (cited supra) in view of Lopriore (cited supra).

33. **Claim 9** is taught by Adams as:

l. *A system, comprising: a memory.* Figure 1 items 14 and 18.

m. *A controller coupled to the memory.* Figure 1 item 16.

n. *And a stack that exists in the memory.* Column 3 lines 54-57 show that stacks are stored within the cache.

o. *Wherein the memory further comprises a cache memory and a main memory.* Figure 1 item 14 is a cache and item 18 is a main memory.

p. *Wherein, if data being removed comprises a predetermined word in a dirty cache line, the controller queues the dirty cache line to be overwritten.* Adams at column 4 line 66 through column 5 line 6 shows that if the data word to be popped is the highest address word in the cache line, the other words in the cache line are necessarily invalid, and the processor is instructed to invalidate the cache line. When the cache line is invalidated, it is left empty and made available for other valid data.

34. Adams teaches that if the data word to be POPPED is the highest address word in the cache line, that word is the last possible word to be POPPED in that particular cache line and the entire cache line is invalidated (column 5 lines 2-4). Adams also states that the cache line is made available for other valid data (column 5 lines 4-6)

Adams makes no exceptions for dirty/not dirty lines. However, Adams does not explicitly teach that a dirty cache line is invalidated, or that the invalidated cache line is not written to memory.

35. With respect to claim 9, Lopriore teaches:

q. *And wherein the dirty cache line is not saved to the main memory*. In the third paragraph of the second column of page 547, which continues on page 548, Lopriore states "*when the stack shrinks, the cache lines reserved for the discarded stack portions at the stack top become free. The cache contains no valid information for these lines, so we do not have to copy the contents of these lines to the primary memory*"

36. Adams and Lopriore are analogous art because they are from the same field of endeavor, computer data cache design.

37. At the time of the invention it would have been obvious to a person of ordinary skill in the art to not write a dirty cache line to main memory when the highest address word in the cache line is POPPED, as the cache line does not contain any valid data (Adams column 5, lines 2-4; Lopriore page 547, second column, line 39 through page 548, first column, line 2).

38. The motivation for doing so would have been to save unnecessary writes to main memory (Lopriore page 547, second column, lines 1-14; also a goal of Adams, column 1 line 54 through column 2 line 11).

39. Therefore, it would have been obvious to combine Lopriore with Adams for the benefit of eliminating unnecessary memory cycles to obtain the invention as specified in claims 9-14 and 16.

40. **Claim 10** is taught by Adams as:

r. *The system of claim 9, wherein the predetermined word is the first word in the dirty cache line.* Column 4 line 66 to column 5 line 6 shows that if the popped data word is the highest address word in the cache line, the processor invalidates the cache line. As shown in figure 2, in the direction of a push operation the highest address word is first in the cache line.

41. **Claim 11** is taught by Adams as:

s. *The system of claim 10, wherein the controller queues the dirty cache line to be overwritten by invalidating the dirty cache line.* Column 5 lines 2-4 show that the cache line is invalidated.

42. **Claim 14** is taught by Adams as:

t. *The system of claim 9, wherein the predetermined word is the last word in the dirty cache line.* Column 4 line 66 to column 5 line 6 shows that if the popped data word is the highest address word in the cache line, the processor invalidates the cache line. As shown in figure 2, in the direction of a pop operation the highest address word is the last word in the cache line.

43. **Claim 16** is taught by Adams as:

u. *The system of claim 9, wherein the dirty cache line is invalidated if the predetermined word in the dirty cache line is the first word.* Column 4 line 66 to column 5 line 6 shows that if the popped data word is the highest address word in the cache line, the processor invalidates the cache line. As shown in figure 2, in the direction of a push operation the highest address word is first in the cache line.

44. **Claim 17** is taught by Adams as:

v. *A system, comprising: a processor that executes stack-based instructions.* Column 1 lines 55-58.

w. *A cache controller coupled to the processor.* Stack cache support logic 16, see column 4 lines 38-42.

x. *And a cache memory coupled to and controlled by said cache controller.* Figure 1 item 14.

y. *Said cache memory storing at least a portion of a stack.* Column 3 lines 54- 57 shows that stacks are stored within the cache.

z. *Said stack having a top and a read access of the stack causes the top of the stack to be read.* Column 1 lines 26-32.

aa. *Wherein, if the processor reads a value from the top of the stack that comprises a word at a predetermined location within a dirty cache line in said*

cache memory, the cache controller queues said dirty cache line for replacement. Adams at column 4 line 66 through column 5 line 6 shows that if the data word to be popped is the highest address word in the cache line, the other words in the cache line are necessarily invalid, and the processor is instructed to invalidate the cache line. When the cache line is invalidated, it is left empty and made available for other valid data.

45. Adams teaches that if the data word to be POPPED is the highest address word in the cache line, that word is the last possible word to be POPPED in that particular cache line and the entire cache line is invalidated (column 5 lines 2-4). Adams also states that the cache line is made available for other valid data (column 5 lines 4-6). Adams makes no exceptions for dirty/not dirty lines. However, Adams does not explicitly teach that a dirty cache line is invalidated, or that the invalidated cache line is not written to memory.

46. With respect to claim 17, Lopriore teaches:

bb. *And the dirty cache line is not written to a memory external to the processor.* In the third paragraph of the second column of page 547, which continues on page 548, Lopriore states "*when the stack shrinks, the cache lines reserved for the discarded stack portions at the stack top become free. The cache contains no valid information for these lines, so we do not have to copy the contents of these lines to the primary memory*"

47. Adams and Lopriore are analogous art because they are from the same field of endeavor, computer data cache design.

48. At the time of the invention it would have been obvious to a person of ordinary skill in the art to not write a dirty cache line to main memory when the highest address word in the cache line is POPPED, as the cache line does not contain any valid data (Adams column 5, lines 2-4; Lopriore page 547, second column, line 39 through page 548, first column, line 2).

49. The motivation for doing so would have been to save unnecessary writes to main memory (Lopriore page 547, second column, lines 1-14; also a goal of Adams, column 1 line 54 through column 2 line 11).

50. Therefore, it would have been obvious to combine Lopriore with Adams for the benefit of eliminating unnecessary memory cycles to obtain the invention as specified in claims 17-20.

51. **Claim 18** is taught by Adams as:

cc. *The system of claim 17 wherein said predetermined location is selected from a group consisting of the first word and the last word of the line.* Column 4 line 66 to column 5 line 6 shows that if the popped data word is the highest address word in the cache line, the processor invalidates the cache line. As shown in figure 2, in the direction of a pop operation the highest address word is the last word in the cache line.

52. **Claim 20** is taught by Adams as:

dd. *The system of claim 17, wherein the cache controller queues the dirty cache line for replacement by invalidating the dirty cache line.* Column 5 lines 2-4 show that the cache line is invalidated.

53. **Claims 12, 13, and 19** are rejected under 35 U.S.C. 103(a) as being unpatentable over Adams, III et al. (cited supra) in view of Lopriore (cited supra) and further in view of Handy (cited supra).

54. **Claim 12** is taught by the combination of Adams and Lopriore as shown supra with respect to claim 11.

55. Although the combination of Adams and Lopriore teaches that the dirty cache line is made available for other valid data (Adams column 5 lines 4-6), the combination of Adams and Lopriore does not explicitly teach queuing the invalidated cache line for replacement by a least-recently-used replacement policy.

56. With respect to claim 12, Handy teaches:

ee. *The system of claim 11, wherein the invalidated cache line is queued for to be overwritten by a least-recently-used (LRU) replacement policy.* At page 57 lines 3-14, Handy teaches that if the cache is a multi-way cache, an algorithm must be used to select a line to be replaced. Page 57 lines 10-14 teaches the use of a LRU replacement algorithm.

57. The combination of Adams and Lopriore and Handy are analogous art because they are from the same field of endeavor, computer data cache design.

58. At the time of the invention it would have been obvious to use a multi-way set associative cache with a least-recently-used replacement policy in the system of Adams and Lopriore.

59. The motivation for using a multi-way set associative cache doing so would have been to lessen thrashing while still improving the hit rate over a direct mapped cache, Handy page 54 lines 1-18. The motivation for using a LRU replacement policy would have been that a processor is much more likely to need to access a memory location which it accessed ten cycles ago than one which it accessed ten thousand cycles ago, Handy page 7 lines 18-22. By replacing the least recently used cache line, a LRU replacement policy reduces the likelihood of evicting data that the processor will need.

60. Therefore it would have been obvious to combine Handy with the combination of Adams and Lopriore for the benefit of reducing thrashing while improving hit rate to obtain the invention as specified in **claim 12**.

61. **Claims 13 and 19** are taught by the combination of Adams and Lopriore as shown supra with respect to claims 9 and 17, respectively.

62. Although the combination of Adams and Lopriore teaches that the dirty cache line is made available for other valid data (Adams column 5 lines 4-6), the combination of Adams and Lopriore does not explicitly teach that the controller designates the dirty cache line as the least recently used cache line.

63. With respect to claims 13 and 19, Handy teaches:

ff. *Wherein the controller queues the dirty cache line to be overwritten by designating the dirty cache line as the least-recently-used (LRU) cache line.* Page 57 lines 9-10 state "*Ideally, any stale piece of cached data which is no longer needed by the processor would be chosen to be overwritten.*" As the cache line is invalidated when the highest address word in the cache line is popped, that cache line no longer contains data which is needed by the processor.

64. The combination of Adams and Lopriore and Handy are analogous art because they are from the same field of endeavor, computer data cache design.

65. At the time of the invention, it would have been obvious to one of ordinary skill in the art to designate the invalidated dirty cache line for replacement.

66. The motivation for doing so would have been to prevent evicting useful data, which may still be useful to the processor, from the cache.

67. Therefore, it would have been obvious to combine Handy with the combination of Adams and Lopriore for the benefit of avoiding evicting useful data to obtain the invention as specified in **claims 13 and 19**.

Response to Arguments

68. Applicant's arguments with respect to claims 1, 9, and 17 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

69. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jared I. Rutz whose telephone number is (571) 272-5535. The examiner can normally be reached on M-F 8:00 AM - 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on (571) 272-4201. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Jared I Rutz
Examiner
Art Unit 2187

jir

Brian R. Peugh
Primary Examiner
2/27/07